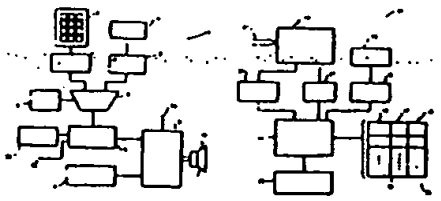
(54) CIPHER SYSTEM
(11) 60-263544 (A) (43) 27.12.1985 (19) JP
(21) Appl. No. 59-119630 (22) 11.6.1984
(71) NIPPON DENSHIN DENWA KOSHA (72) TEIZOU NAGAMINE(1)
(51) Int. Cl⁴. H04L9/00,G06F12/14,G09C1/00

PURPOSE: To improve the cipher capacity of a password by combining a password, a function number and time information together to obtain the ciphered key information and transmitting this information together with a member number.

CONSTITUTION: A function number given to a member having a cipher transmitter 11 is stored in a function number register 3 together with the member number stored in a member number register 7. While the present time information sent from a timepiece circuit 4 is stored in a time information register 2 respectively. A member pushes a matrix key 9 to store a password registered previously in a password register 1. A function device 5 uses the password, the function number and the time information to perform an operation with a prescribed algorithm. Thus the key information is produced and stored in a key information register 6. The information on registers 6 and 7 are transmitted via a PB transmission circuit 8 and an acoustic coupler speaker 10. The key information is separated from the member number at the reception side. A password check circuit 14 detects a password and a function number out of a member number table 15, and the key information is reproduced from the present time information for check of the propriety.

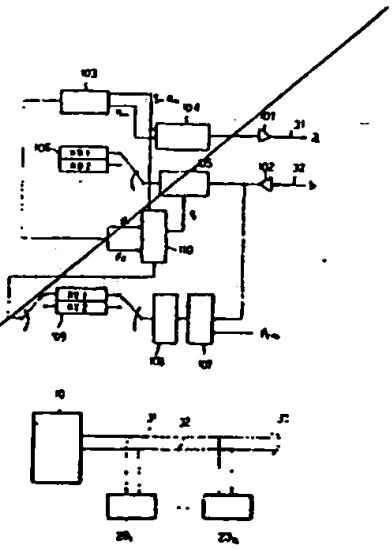


12: time information register, 13: timepiece circuit, 16: member No., 17: password, 18: secret No., 19: PB signal reception circuit, 20: key information register, 21: member No. register, 22: check information store register, 23: memory, 24: circuit input terminal

(54) MULTIPLEX TRANSMISSION SYSTEM
(11) 60-263545 (A) (43) 27.12.1985 (19) JP
(21) Appl. No. 59-119704 (22) 11.6.1984
(71) NIPPON DENSHIN DENWA KOSHA (72) TERUYUKI KUBO(3)
(51) Int. Cl⁴. H04L11/00

PURPOSE: To decide the optimum signal identifying timing corresponding to a reception channel through a main device, by calculating the arriving time point of an ascending channel based on the phase of a transmission frame and producing a signal identifying clock.

CONSTITUTION: A main device 10 is connected in a multiple way to plural slave devices 20_1–20_n via a common transmission line 30 and then assembles plural descending channels CH into a frame through a transmission frame assembling circuit 104. This frame is sent to a descending transmission line 31 via a driver 101. Each slave device identifies the phase of the frame and transmits in time division the signals of ascending CH to an ascending transmission line 32 with the allocated phase. The device 10 receives this signal by a receiver 102 and counts plural times a time point when the ascending CH arrives by a time counting circuit 107 and based on the phase of a transmission frame. When coincidence is obtained among those time counting actions, a coincidence deciding circuit 108 regards this coincident value as significant and sends this count value to a timing register 109. An identifying clock source 110 sends an identifying clock having a phase corresponding to the ascending CH to an identifying circuit 105 according to the count value of the register 109 and identifies the reception signals.

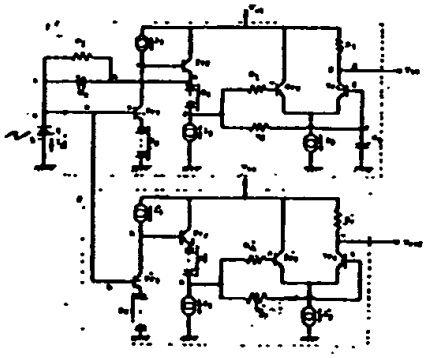


103: main clock source, a: R line, b: T line

(54) REFERENCE POTENTIAL GENERATING CIRCUIT OF LIGHT RECEPTION CIRCUIT
(11) 60-263546 (A) (43) 27.12.1985 (19) JP
(21) Appl. No. 59-118929 (22) 9.6.1984
(71) SUMITOMO DENKI KOGYO K.K. (72) TAKANORI SAWAI
(51) Int. Cl⁴. H04L25/06,G08C23/00,H04B9/00

PURPOSE: To set a reference potential equal to the mean level of a differential signal by providing a reference potential generating part excluding a signal transmission part within a circuit that converts the current flowing to a photodetecting element into the voltage and differentiating and amplifying said voltage.

CONSTITUTION: The current flowing to a photodetecting element 1 receiving the digital optical signal is converted into the voltage by a resistance R_1 and transistors Tr1 and 2. This voltage is amplified by a differential amplifier consisting of Tr3 and 4 via a delay circuit consisting of a resistance R_2 and a capacitor C_1. Then a signal V_{os} is delivered. The capacitor C_1 repeats charging and discharging with blinking of the light applied to the element 1. A signal V_{os} is equal to a signal obtained by differentiating the voltage that converted the current of the element 1. A reference potential generating part 3 has the same constitution as an amplifying part 2 excepting the signal transmission parts of the R_1 and the C_1 of the part 2. The new voltage is always applied to the bases S and T of the differential amplifying Tr3 and 4 of the part 3. Then an equal current flows to both Tr3 and 4. The reference potential Vref outputted from the collector of the Tr4 is equal to the mean value of the signal V_{os}.



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		6914-5K	H 04 L 9/00 A

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